

**INFORMATION DISCLOSURE  
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Application Number	09/592,106
Filing Date	06/12/2000
First Named Inventor	Stephen Melvin
Art Unit	2154
Examiner Name	Larry D. Donaghue
Attorney Docket Number	P3813

**U. S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Document Number Number-Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
S		US- 5600837 A *	02-04-1997	Artieri, Alain	
S		US- 5461722 A *	10-24-1995	Goto, Tatsuhiro	
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S		US- 5748468 A *	05-05-1998	Notenboom et al.	
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Examiner Name	Larry D. Donaghue

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## NON PATENT LITERATURE DOCUMENTS

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<i>SD</i>	*	FISKE et al., "Thread Prioritization: A Thread Scheduling Mechanism for Multiple-Context Parallel Processors", 1995, pp 210 -221, IEEE	
<i>W</i>	*	YAMAMOTO, Wayne, "An Analysis of Multistreamed, Superscalar Processor Architectures", University of California Santa Barbara dissertation, December 1995, Santa Barbara, US	
<i>M</i>	*	STEERE et al., "A Feedback - Driven Proportion Allocator for Real-Rate Scheduling", Third Symposium on Operating Systems Design and Implementation, February 1999, pp.145-158, USENIX Association	
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<i>J</i>	*	KESSLER, R.E., "The Alpha 21264 Microprocessor: Out-of-Order Execution at 600 Mhz", August 1998	
<i>TD</i>	*	YAMAMOTO ET AL., Performance Estimation of Multistreamed, Superscalar Processors, IEEE. 1994, pp 195-204, Hawaii, US	
<i>O</i>	*	NEMIROVSKY et al., "Quantitative Study of Data Caches on a Multistreamed Architecture", Workshop on Multithreaded Execution Architecture and Compilation, January 1998	
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Application Number	09/592,106	RECEIVED
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First Named Inventor	Stephen Melvin	
Art Unit	2154	
Examiner Name	Larry D. Donaghue	Technology Center 2000
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<i>S</i>		* The PowerPC Architecture: A Specification for a New Family of RISC Processors, Second Edition, May 1994, pp 70-72, Morgan Kaufmann, San Francisco	
<i>S</i>		* MC68020 32-Bit Microprocessor User's Manual, Third Edition, 1989, pp 3-125, 3-126, and 3-127, Prentice Hall, New Jersey	
<i>S</i>		* POTEI, M.J., Real-Time Playback in Animation Systems, Proceedings of the 4th Annual Conference on Computer Graphics and Interactive Techniques, 1977, pp. 72-77, San Jose, CA	
<i>S</i>		* ARM Architecture Reference Manual, 1996, pp. 3-41, 3-42, 3-43, 3-67, 3-68, Prentice Hall	
<i>S</i>		* ESA/390 Principles of Operation, IBM Library Server, 1993, Table of Contents and Para. 7.5.31 and 7.5.70 (available at : <a href="http://publibz.boulder.ibm.com/cgi-bin/bookmgr_OS390/BOOK/DZ9AR001/CCONTENTS">http://publibz.boulder.ibm.com/cgi-bin/bookmgr_OS390/BOOK/DZ9AR001/CCONTENTS</a> )	
<i>S</i>		* MC88110 Second Generation RISC Microprocessor User's Manual, 1991, pp. 10-66, 10-67 and 10-71, Motorola, Inc.	
<i>S</i>		* DIEFENDORFF, KEITH et al., Organization of the Motorola 88110 Superscalar RISC Microprocessor, IEEE Micro, April 1992, pp.40-63, Vol. 12, No. 2	
<i>S</i>		* KANE, GERRY, PA-RISC 2.0 Architecture, 1996, pp 7-106 and 7-107, Prentice Hall, New Jersey	
<i>S</i>		* DIEFENDORFF, KEITH et al., AltiVec Extension to PowerPC Accelerates Media Processing, March - April 2000, pp. 85-95, IEEE Micro, Vol. 20, No. 2	
<i>S</i>		* NEMIROVSKY ET AL., DISC: Dynamic Instruction Stream Computer, ACM, 1991, pp 163-171	

Examiner Signature	<i>S</i>	Date Considered	07/18/01
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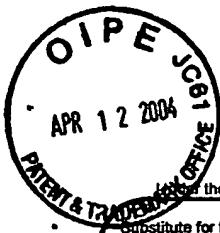
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				<b>Filing Date</b> <u>06/12/00</u>		
				<b>First Named Inventor</b> <u>Stephen Melvin Mario D. Nemirovsky</u>		
				<b>Group Art Unit</b> <u>2154</u>		
				<b>Examiner Name</b> <u>Larry D. Donaghue</u>		
<b>Sheet</b>	<b>1</b>	<b>of</b>	<b>1</b>	<b>Attorney Docket Number</b> <u>MIPS.0167-00-US</u>		

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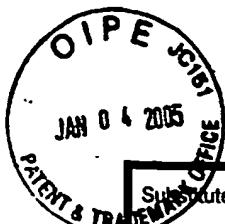
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<i>g</i>	AA	DIEFENDORFF, KEITH, "WinChip 4 Thumbs Nose at ILP," <i>Microprocessor Report</i> , Vol. 12, No.16, 10 pages (December 7, 1998)	
<i>g</i>	AB	EGGERS ET AL, "Simultaneous Multithreading: A Platform for Next-Generation Processors", <i>IEEE Micro</i> , 1997.	
<i>g</i>	AC	DIEFENDORFF, KEITH; "Jalapeno Powers Cyrix's M3", <i>Microprocessor Report</i> , Vo. 12, No. 15, Nov. 16, 1998.	
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<i>g</i>	AG	POTEL, M.J., "Real-time Playback in Animation Systems", Proceedings of the 4 <sup>th</sup> Annual Conference on Computer Graphics and Interactive Techniques, 1977, pp.72-77, San Jose, CA.	
<i>g</i>	AH	ARM Architecture Reference Manual, 1996, pp.3-41, 3-42, 3-43, 3-67, 3-68, Prentice Hall.	
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<i>g</i>	AO	STEERE et al, "A Feedback-Driven Proportion Allocator for Real Estate Scheduling", Third Symposium on Operating Systems Design and Implementation, February 1999, pp.145-158, USENIX Association.	

Examiner Signature

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